Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-41 are pending in the application, of which claims 1, 11, 20, 27, 30, and 38 are independent. Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Objection to the Specification

The Examiner, on page 2 of the Office Action, has requested that blank spaces be filled with the proper serial numbers in the Specification of the application. Applicants have amended the Specification to fill in each blank space with the appropriate serial number(s). Applicants respectfully request that the Examiner review the amendments to the Specification and withdraw this objection.

Rejections under 35 U.S.C. § 103

The Examiner, on page 3 of the Office Action, has rejected claims 1-41 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,285,779 to Lapidous *et al.* (hereinafter "Lapidous") in view of "MIPS R4000 Microprocessor User's Manual" by J. Heinrich (hereinafter "Heinrich"). Applicants respectfully traverse this rejection. Based on the remarks set forth below, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The Examiner states that Lapidous discloses the claimed features of applicants' invention with respect to claim 1, except that Lapidous does not explicitly disclose the processing of floating point compare operations. The Examiner further states that the processing of floating point compare operations are taught by Heinrich.

Applicants agree that Lapidous does not disclose the processing of floating point compare operations. However, Applicants respectfully disagree that Heinrich teaches this feature.

Heinrich does not solve the deficiencies of Lapidous. The present invention uses "a floating point magnitude compare instruction to perform a floating point magnitude comparison" as recited in claim 1. The floating point magnitude compare instruction takes two input values specified by the instruction and compares their absolute values using the compare condition specified in the instruction.

Contrary to the present invention, Heinrich does not teach or suggest a floating point magnitude compare instruction. Instead, Heinrich teaches a floating point compare of the actual values of the two input values, which includes their sign.

Thus, neither Lapidous nor Heinrich, separately or in combination, teach or suggest Applicants' claimed invention of "a floating point magnitude compare instruction to perform a floating point magnitude comparison" as recited in independent claim 1. For at least the reasons stated above, claim 1 and the claims that depend therefrom (claims 2-10 and 40) are patentable over the cited references of Lapidous and Heinrich. Independent claims 11, 20, 27, 30, and 38 also include the feature of "a floating point magnitude compare instruction" or "magnitude compare operation(s)". Thus, for at least the reasons stated above, independent claims 11, 20, 27, 30, and 38 and the claims that depend therefrom (claims 12-

19 and 41, claims 21-26, claims 28-29, claims 31-37, and claim 39, respectively) are also patentable over the cited references. Applicants therefore respectfully request that the Examiner reconsider and withdraw the rejection of claims 1-41.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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Date: 10/18/02

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Version with markings to show changes made

In the Specification

Please substitute the paragraph beginning on page 1, line 7, with the following paragraph:

U.S. Patent Application No. [_____ (Attorney Docket No. 1778.0080000)] 09/363,637; inventors Ying-wai Ho, Michael Schulte and John Kelley; and entitled "System and Method for Improving the Accuracy of Reciprocal and Reciprocal Square Root Operations Performed by a Floating-Point Unit;"

Please substitute the paragraph beginning on page 1, line 12, with the following paragraph:

U.S. Patent Application Serial No. [_____ (Attorney Docket No. 19427-89-1)] 09/364,514; inventors John Kelley and Ying-wai Ho; and entitled "Floating-Point Processor With Improved Intermediate Result Handling;"

Please substitute the paragraph beginning on page 1, line 16, with the following paragraph:

U.S. Patent Application Serial No. [_____ (Attorney Docket No. 19427A-007520)] 09/364,787; inventors Radhika Thekkath, Michael Uhler, Ying-wai Ho, and Chandlee Harrell; and entitled "Processor Having an Arithmetic Extension of an Instruction Set Architecture;"

Please substitute the paragraph beginning on page 1, line 21, with the following paragraph:

U.S. Patent Application Serial No. [_____ (Attorney Docket No. 19427A-007820)] 09/364,789; inventors Radhika Thekkath, Michael Uhler, Ying-wai Ho, and Chandlee Harrell; and entitled "Processor Having a Conditional Branch Extension of an Instruction Set Architecture;"

Please substitute the paragraph beginning on page 2, line 2, with the following paragraph:

U.S. Patent Application Serial No. [_____ (Attorney Docket No. 19427-97)] 09/364,512; inventors Ying-wai Ho, John Kelley and James Jiang; and entitled "Processor With Improved Accuracy For Multiply-Add Operations;" and

Please substitute the paragraph beginning on page 2, line 6, with the following paragraph:

U.S. Patent Application Serial No. [_____ (Attorney Docket No. 1778.0060000)] 09/363,638; inventors James Jiang, Ying-wai Ho and John Kelley; and entitled "Method and Apparatus for Predicting Floating-Point Exceptions."

Please substitute the paragraph beginning on page 29, line 1, with the following paragraph:

Floating point adder 284 is a floating point mantissa adder which implements single precision, double precision, and paired-single floating point add instructions (e.g.,

ADDR of Table 1) and subtract instructions, as well as the add/subtract portions of compound instructions such as MADD (i.e., floating point multiply add, described below). Floating point adder 284 accepts two operands, an intermediate result from floating point multiplier 283 and a mantissa staged in floating point pipe file 282. To increase performance, a floating-point magnitude addition/subtraction operation is computed by either a prescale adder (PSA) 583 or a massive cancellation adder (MCA) 584 (Figure 2D). PSA 583 performs all magnitude additions and often performs magnitude subtractions if the difference in operand exponents is greater than two (2), thereby avoiding a large normalization shift after the operation. MCA 584 often performs magnitude subtractions if the difference in operand exponents is less than or equal to two (2), thereby avoiding a large alignment shift before the operation. Thus, the final correct result is selected from either PSA 583 or MCA 584 based upon, among other things, the exponential difference of the operands. The result is then returned to floating point pipe file 282. Selection criteria for PSA 583 and MCA 584 are further described in the above-referenced U.S. Patent Application Serial No. [_____ (Attorney Docket No. 19427-97)] 09/364,512.

Please substitute the paragraph beginning on page 32, line 6, with the following paragraph:

Referring to Figure 2D, data start from floating point register file 281 passing from register 502 (32-entry, 64-bit register file with 4 read ports and 2 write ports) to unpack/bypass logic 508 in pipe file 282. (Data may also flow directly into logic 508 from load bus 291 and register file 507.) This logic unpacks an operand into an "internal

format," discussed in previously-identified copending [applications _____ (Attorney Docket Nos. 1778.0060000 and 1778.0080000)] application nos. 09/363,638 and 09/363,637 . This logic may also perform bypass operations for operands that do not require any arithmetic operation (i.e., circulate operands back to file 281). Where arithmetic operation is required, data then flow to multiplier 283 and exponent 286.

Please substitute the paragraph beginning on page 33, line 16, with the following paragraph:

Further discussion of FPU 270 and alternative embodiments are provided in the previously identified copending [applications _____ (Attorney Docket Nos. 19427-89-1, 19427-97, 1778.0060000, and 1778.0080000)] application nos. 09/364,514, 09/364,512, 09/363,638, and 09/363,637.

Please substitute the paragraph beginning on page 36, line 18, with the following paragraph:

An alternative embodiment of FCSR 410 is provided in previously-identified copending application [_____ (Attorney Docket No. 19427-97)] no. 09/364,512. In this embodiment, an additional control bit "FO" (Madd-flush-override bit) is provided to the FCSR. The combination of bits FS and FO enable an FPU (such as FPU 270) to selectively operate in up to three different modes; i.e., IEEE-compliant, Flush-to-zero and Madd-flush-override.

Please substitute the paragraph beginning on page 52, line 18, with the following paragraph:

Equation (1) results in a term "(2 - bx_i)" which is frequently close to 1.0 (such as 1.0000...nnnn..., where nnnn is the correction adjustment and the number of interest). This format can result in a loss of precision. In contrast, in equation (2), the term "(1 - bx_i)" is first determined (using RECIP2 604). By subtracting 1.0 in RECIP2 604, the resulting number is typically very small and can be normalized (as n.nnn...) to achieve greater precision. Therefore, subsequent calculations are more precise and denormalization may be avoided. This technique is further discussed in copending application [_____ (Attorney Docket No. 1778.0080000)] no. 09/363,637.

Please substitute the paragraph beginning on page 64, line 1, with the following paragraph:

Equation (3) has a term x_i^2. If b is a very large number, x_i^2 can initially create a denormalized number. In contrast, in equation (4) the term "(1-bx_i*x_i)/2" is determined using RSQRT2 606 in a sequence of instructions (as set out below) where b is first multiplied with x_i. This order of operation can pull the quantity "b*x_i" back to a sufficiently normal range so that subsequent multiplication with x_i may not create denormalization. This technique is further discussed in copending application [_____ (Attorney Docket No. 1778.0080000)] no. 09/363,637. This operation is computed in the pipelines of floating point multiplier 283 and floating point adder 284 of FPU 270 (Figure 2C).